



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Am

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/850,239	05/07/2001	Ruby B. Lee	4759-104 US	2238

7590 06/24/2005

Mathews, Collins, Shepherd & Gould, P.A.
100 Thanet Circle, Suite 306
Princeton, NJ 08540

EXAMINER

CALLAHAN, PAUL E

ART UNIT PAPER NUMBER

2137

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/850,239

Applicant(s)

LEE ET AL.

Examiner

Paul Callahan

Art Unit

2137

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-57 and 66-77 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8-19, 32-57 and 66-77 is/are allowed.
- 6) ☒ Claim(s) 1-3, 7, 20, 25-27 and 31 is/are rejected.
- 7) ☒ Claim(s) 4-6, 21-24 and 28-30 is/are objected to.
- 8) ☐ Claim(s) 58-65 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 May 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)

Paper No(s)/Mail Date PC

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

2

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Claim group I, composed of claims 1-57 and 66-77 in the reply filed on 1-25-2005 is acknowledged. The traversal is on the ground(s) that a search of the method of Group 1 would uncover a computer system of Group 11 and a circuit of Group 111. Applicants respectfully request the right to file a divisional application directed to the unelected claims. This is not found persuasive because groups II and II disclose different inventions not disclosed as usable together or with the invention set forth in claim group I.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 1-57 and 66-77 are pending in this application and have been examined.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1-3, and 7 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Turkowski, US 5,524,256.

As for claim 1 Turkowski teaches a method of performing an arbitrary permutation in a programmable processor (abstract) comprising the steps of:

- a. Defining bit positions in a source sequence of bits to be permuted in a source register for a group of bits in a destination register (fig. 6, col. 2 lines 46-67).
- b. Determining a permutation instruction with said bit positions to assemble bits from said source sequence of bits (col. 4 lines 25-65);
- c. Performing said permutation instruction for inserting said assembled bits into a destination register as determined by said bit positions (col. 4 lines 25-65, col. 6 lines 33-65); and
- d. Repeating steps a. through c. for groups of bits in said destination register, wherein after a final permutation instruction a desired permutation of said source register is determined and said determined permutation instructions form a permutation instruction sequence (col. 6 lines 35-65).

As for claim 2, Turkowski teaches the method of claim 1 wherein step d repeats steps a. through c. for all non overlapping said groups of bits in said destination register

Art Unit: 2137

(col. 4 lines 25-65, col. 6 lines 35-65, col. 7 lines 17-25).

As for claim 3, Turkowski teaches the method of claim 1 wherein said permutation instruction comprises a first parameter indicating which k bits in said destination register will change, a reference to said source register which contains said source sequence of bits to be permuted, a reference to a configuration register which contains configuration bits for indicating which said bits in said source register are assembled and a reference to said destination register (col. 4 lines 25-65).

As for claim 7, Turkowski teaches the method of claim 1 wherein said programmable processor is a microprocessor, digital signal processor, media processor, multimedia processor, cryptographic processor, network processor, or programmable System-on-a-Chip(SOC) col. 7 lines 17-25.

5. Claims 20, 25-27 and 31 are rejected under 35 U.S.C. 102(a) as being clearly anticipated by Cole, 6,865,272.

As for claim 20, Cole teaches a system of performing an arbitrary permutation in a programmable processor (abstract) comprising: means for defining bit positions in a source sequence of bits to be permuted in a source register for a group of bits in a destination register (col. 2 lines 30-55); means for determining permutation instructions with said bit positions to assemble bits from said source sequence of bits into one or more intermediate sequences of bits until a desired sequence is obtained (col. 2 lines

Art Unit: 2137

30-55); means for performing said determined permutation instructions for inserting said assembled bits into a destination register as determined by said bit positions for each of said one or more intermediate sequences of bits or said desired sequence (col. 2 lines 30-55); wherein after a final permutation instruction a desired permutation of said source register is determined and said determined permutation instructions form a permutation instruction sequence (col. 2 lines 30-55).

As for claim 25, Cole teaches the system of claim 20 wherein said programmable processor is a microprocessor, digital signal processor, media processor, multimedia processor, cryptographic processor, network processor, or programmable System-on-a-Chip(SOC) (abstract).

As for claim 26, Cole teaches a system of performing an arbitrary permutation at a source sequence of bits in a programmable processor (abstract) comprising the steps of: means for determining an initial and final arrangement of a source sequence of bits (col. 2 lines 30-55); means for defining one or more intermediate sequence of bits that said initial arrangement of said source sequence of bits is transformed into until a desired sequence is obtained (col. 2 lines 30-55); means for determining permutation instructions for transforming said source sequence of bits into for each of said one or more intermediate sequence of bits or said desired sequence by dividing said arrangement into a first group and a second group and combining said first group and said second group; wherein the determined permutation instructions form a permutation

Art Unit: 2137

instruction sequence (col. 2 lines 30-55).

As for claim 27, Cole teaches the system of claim 26 wherein said permutation instruction comprises a reference to a source register which contains said arrangement, a reference to a configuration register which contains configuration bits and a reference to a destination register to which the intermediate sequence of bits or said desired sequence of bits is placed (col. 2 lines 30-55).

As for claim 31, Cole teaches the system of claim 26 wherein said programmable processor is a microprocessor, digital signal processor, media processor, multimedia processor, cryptographic processor, network processor, or programmable System-on-a-Chip(SOC) (abstract).

Allowable Subject Matter

6. Claims 8-19, 32-57 and 66-77 are allowed.
7. Claim 4-6, 21-24, and 28-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Art Unit: 2137

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E. Callahan whose telephone number is (571) 272-3869. The examiner can normally be reached on M-F from 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Andrew Caldwell, can be reached on (571) 272-3868. The fax phone number for the organization where this application or proceeding is assigned is: (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

6-17-2005

Paul Callahan